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SCHEIBEL, ROBERT C	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/826,158	Applicant(s) WYBENGA ET AL.	
	Examiner Robert C. Scheibel	Art Unit 2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,11-15 and 21-24* is/are rejected.

7)☒ Claim(s) *6-10 and 16-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: in paragraph 006 on page 4, the acronym TCAM should be defined prior to its first use.

Appropriate correction is required.

Claim Objections

2. Claims 1 and 11 are objected to because of the following informalities: the phrase "an address portion of an address" in lines 7-8 of claim 1 and 11-12 of claim 11 is vague. Examiner suggests changing it to something such as "a portion of an address". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims **1-5 and 21-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2004/0114587 to Huang et al in view of "Survey and Taxonomy of IP Address Lookup Algorithms" by Ruiz-Sanchez et al.

Regarding claim **1**, Ruiz-Sanchez discloses a router, a routing table search circuit for determining a first destination address for a first received data packet comprising:

a forwarding table comprising a plurality of forwarding table entries, each of said forwarding table entries comprising a destination address (see the next hop table described in paragraphs 15 and 16 on page 1-2);

a trie tree search table for translating an address portion of an address associated with said first received data packet into a destination pointer for accessing said first destination address in said forwarding table, wherein a first stage of said trie tree search table is searched using a received address pointer retrieved from a previous stage of said trie tree search table and a first m-bit symbol comprising m bits of said address portion (see paragraphs 12-14 on page 1, Figures 2 and 4 and the associated description in paragraphs 68-72 on page 5; these sections clearly disclose that the portion of an address (the search key) is translated by the trie tree into a destination pointer for the forwarding table (next hop table) and that a given stage of the trie tree search table uses multiple bits of the key (each stage consumes n-bits));

at least one consecutive symbols table associated with said first stage of said trie tree search table (see figure 3 and the associated description in paragraphs 46-51 on pages 3-4 which

indicates that the memory banks of Figure 4 are consecutive symbol tables as they contain information (skip count) on how many consecutive symbols (strides or pipeline stages) to skip from the current stage of the pipeline).

Huang does not disclose the control circuit capable of determining that a second m-bit symbol immediately following said first m-bit symbol is the same as said first m-bit symbol, wherein said control circuit, in response to said determination, determines a total number of consecutive identical m-bit symbols beginning with said first m-bit symbol.

However, Ruiz-Sanchez discloses a control circuit capable of determining that a second m-bit symbol immediately following said first m-bit symbol is the same as said first m-bit symbol (see "Compression Techniques" on page 13 which describes replacing "consecutive occurrences of a given symbol with only one occurrence plus a count of how many times the symbol occurs" as a means for compressing the information in trie tree tables) , wherein said control circuit, in response to said determination, determines a total number of consecutive identical m-bit symbols beginning with said first m-bit symbol (in the passage cited above, the consecutive symbols are replaced by one symbol and the number of times the symbol occurs).

Huang and Ruiz-Sanchez are analogous art because they are from the same field of endeavor of trie tree search engines in routers. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Huang to compress the data in the trie tree using the run-length means suggested by Ruiz-Sanchez. The motivation for doing so would have been so that "memory consumption is decreased, and retrieving the information from the compressed structure can be done easily and with a minimum number of memory accesses" as suggested by Ruiz-Sanchez in "Compression Techniques" on page 13. Therefore, it would have

been obvious to combine Ruiz-Sanchez with Huang for the benefit of reducing memory consumption and minimizing memory accesses to obtain the invention as specified in claim 1.

Regarding claim **21**, Huang discloses a method for determining a first destination address for a first received data packet comprising the steps of:

searching a first stage of trie tree search table using a received address pointer retrieved from a previous stage of the trie tree search table and a first m-bit symbol comprising m bits of an address portion of an address associated with the first received data packet (see paragraphs 12-14 on page 1, Figures 2 and 4 and the associated description in paragraphs 68-72 on page 5; these sections clearly disclose that the portion of an address (the search key) is translated by the trie tree into a destination pointer for the forwarding table (next hop table) and that a given stage of the trie tree search table uses multiple bits of the key (each stage consumes n-bits));

retrieving from a consecutive symbols table associated with the first stage of the trie tree search table a first address pointer determined by the total number of consecutive m-bit symbols, wherein the first address pointer may be used to access the first destination address in a forwarding table of the router (see figure 3 and the associated description in paragraphs 46-51 on pages 3-4 which indicates that the memory banks of Figure 4 are consecutive symbol tables as they contain information (skip count) on how many consecutive symbols (strides or pipeline stages) to skip from the current stage of the pipeline; Huang discloses that the skip count is retrieved from this table and that a pointer to the forwarding table (next hop table) may be obtained (paragraph 15)).

Huang does not disclose the limitations of determining that a second m-bit symbol immediately following the first m-bit symbol is the same as the first m-bit symbol; or that in

response to the determination, determining a total number of consecutive identical m-bit symbols beginning with the first m-bit symbol.

However, Ruiz-Sanchez discloses the use of run-length compression in trie tree tables. Specifically, Ruiz-Sanchez discloses the advantages of using "a very simple compression technique that replaces consecutive occurrences of a given symbol with only one occurrence plus a count of how many times the symbol occurs". This discloses both determining that a second m-bit symbol immediately following the first m-bit symbol is the same as the first m-bit symbol ("consecutive occurrences of a given symbol"); and in response to the determination, determining a total number of consecutive identical m-bit symbols beginning with the first m-bit symbol ("a count of how many times the symbol occurs").

Huang and Ruiz-Sanchez are analogous art because they are from the same field of endeavor of trie tree search engines in routers. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Huang to compress the data in the trie tree using the run-length means suggested by Ruiz-Sanchez. The motivation for doing so would have been so that "memory consumption is decreased, and retrieving the information from the compressed structure can be done easily and with a minimum number of memory accesses" as suggested by Ruiz-Sanchez in "Compression Techniques" on page 13. Therefore, it would have been obvious to combine Ruiz-Sanchez with Huang for the benefit of reducing memory consumption and minimizing memory accesses to obtain the invention as specified in claim 21.

Regarding claim **2**, Huang discloses the limitation that said control circuit retrieves from said at least one consecutive symbols table a first address pointer determined by said total

number of consecutive m-bit symbols (the pointer field in Figure 3C; see paragraphs 75 and 76 on page 6 for a description of how the pointer is determined by the number of consecutive m-bit symbols (skip count)).

Regarding claim **3**, Huang discloses the limitation that said first address pointer comprises said destination pointer (see paragraph 15 on pages 1-2 which describes that the pointer points to a location in the next hop table when at an end-node).

Regarding claim **4**, Huang discloses the limitation that said first address pointer is used to search a subsequent stage of said trie tree search table (see paragraph 16 on page 2 and paragraph 75 on page 6 which indicate that at other times the pointer points to one of the next stages in the trie tree table).

Regarding claim **5**, Huang discloses the limitation that said at least one consecutive symbols table comprises a plurality of consecutive symbols tables and said control circuit uses a value of said first m-bit symbol to select a first one of said plurality of consecutive symbols tables (there is a separate trie tree as well as a separate consecutive symbols table (memory bank) for every branch/child in a given stage (see paragraph 14, for example) and the particular child table is selected based on the value of the m-bit symbol evaluated a the parent node).

Regarding claim **22**, Huang discloses accessing the first destination address in the forwarding table using the first address pointer (see paragraph 15 on pages 1-2 which describes that the pointer points to a location in the next hop table when at an end-node).

Regarding claim **23**, Huang discloses searching a subsequent stage of the trie tree search table using the first address pointer (see paragraph 16 on page 2 and paragraph 75 on page 6

which indicate that at other times the pointer points to one of the next stages in the trie tree table).

Regarding claim **24**, Huang discloses the consecutive symbols table comprises a plurality of consecutive symbols tables and further comprising the step of selecting a first one of the plurality of consecutive symbols tables according to a value of the first m-bit symbol (there is a separate trie tree as well as a separate consecutive symbols table (memory bank) for every branch/child in a given stage (see paragraph 14, for example) and the particular child table is selected based on the value of the m-bit symbol evaluated a the parent node).

6. Claims **11-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2004/0114587 to Huang et al in view of "Survey and Taxonomy of IP Address Lookup Algorithms" by Ruiz-Sanchez et al and in further view of U.S. Patent 6,496,510 to Tsukakoshi et al.

Regarding claim **11**, Ruiz-Sanchez discloses a routing node comprising a routing table search circuit for determining a first destination address for a first received data packet comprising:

a forwarding table comprising a plurality of forwarding table entries, each of said forwarding table entries comprising a destination address (see the next hop table described in paragraphs 15 and 16 on page 1-2);

a trie tree search table for translating an address portion of an address associated with said first received data packet into a destination pointer for accessing said first destination address in said forwarding table, wherein a first stage of said trie tree search table is searched

using a received address pointer retrieved from a previous stage of said trie tree search table and a first m-bit symbol comprising m bits of said address portion (see paragraphs 12-14 on page 1, Figures 2 and 4 and the associated description in paragraphs 68-72 on page 5; these sections clearly disclose that the portion of an address (the search key) is translated by the trie tree into a destination pointer for the forwarding table (next hop table) and that a given stage of the trie tree search table uses multiple bits of the key (each stage consumes n-bits));

at least one consecutive symbols table associated with said first stage of said trie tree search table (see figure 3 and the associated description in paragraphs 46-51 on pages 3-4 which indicates that the memory banks of Figure 4 are consecutive symbol tables as they contain information (skip count) on how many consecutive symbols (strides or pipeline stages) to skip from the current stage of the pipeline).

Huang does not disclose the control circuit capable of determining that a second m-bit symbol immediately following said first m-bit symbol is the same as said first m-bit symbol, wherein said control circuit, in response to said determination, determines a total number of consecutive identical m-bit symbols beginning with said first m-bit symbol.

Huang also does not disclose the limitation that the router is comprised of a switch fabric and a plurality of routing nodes coupled to the switch fabric.

However, Ruiz-Sanchez discloses a control circuit capable of determining that a second m-bit symbol immediately following said first m-bit symbol is the same as said first m-bit symbol (see "Compression Techniques" on page 13 which describes replacing "consecutive occurrences of a given symbol with only one occurrence plus a count of how many times the symbol occurs" as a means for compressing the information in trie tree tables) , wherein said

control circuit, in response to said determination, determines a total number of consecutive identical m-bit symbols beginning with said first m-bit symbol (in the passage cited above, the consecutive symbols are replaced by one symbol and the number of times the symbol occurs).

Huang and Ruiz-Sanchez are analogous art because they are from the same field of endeavor of trie tree search engines in routers. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Huang to compress the data in the trie tree using the run-length means suggested by Ruiz-Sanchez. The motivation for doing so would have been so that "memory consumption is decreased, and retrieving the information from the compressed structure can be done easily and with a minimum number of memory accesses" as suggested by Ruiz-Sanchez in "Compression Techniques" on page 13.

Huang and Ruiz-Sanchez do not disclose the limitation that the router is comprised of a switch fabric and a plurality of routing nodes coupled to the switch fabric. However, this type of router architecture is well-known in the art. Consider Tsukakoshi, for example, which in Figure 1 discloses a switch fabric (element 13), and a plurality of routing nodes coupled to said switch fabric (router nodes 12).

Huang and Tsukakoshi are analogous art because they are from the same field of endeavor of router architecture. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use modify the router in the combination of Huang and Ruiz-Sanchez to use a distributed "cluster-type" architecture as in Tsukakoshi. The motivation for doing so would have been to allow for a scalable architecture allowing for much higher performance in routing higher and higher rates of data. Therefore, it would have been obvious to

combine Tsukakoshi with Huang and Ruiz-Sanchez for the benefit of a scalable architecture to obtain the invention as specified in claim 11.

Regarding claim **12**, Huang discloses the limitation that said control circuit retrieves from said at least one consecutive symbols table a first address pointer determined by said total number of consecutive m-bit symbols (the pointer field in Figure 3C; see paragraphs 75 and 76 on page 6 for a description of how the pointer is determined by the number of consecutive m-bit symbols (skip count)).

Regarding claim **13**, Huang discloses the limitation that said first address pointer comprises said destination pointer (see paragraph 15 on pages 1-2 which describes that the pointer points to a location in the next hop table when at an end-node).

Regarding claim **14**, Huang discloses the limitation that said first address pointer is used to search a subsequent stage of said trie tree search table (see paragraph 16 on page 2 and paragraph 75 on page 6 which indicate that at other times the pointer points to one of the next stages in the trie tree table).

Regarding claim **15**, Huang discloses the limitation that said at least one consecutive symbols table comprises a plurality of consecutive symbols tables and said control circuit uses a value of said first m-bit symbol to select a first one of said plurality of consecutive symbols tables (there is a separate trie tree as well as a separate consecutive symbols table (memory bank) for every branch/child in a given stage (see paragraph 14, for example) and the particular child table is selected based on the value of the m-bit symbol evaluated a the parent node).

Allowable Subject Matter

7. Claims **6-10 and 16-20** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- U.S. Patent 6,192,051 to Lipman et al discloses a network router search engine using a compressed tree forwarding table.
- U.S. Patent 6,697,363 to Carr discloses a method for longest matching prefix determination.
- U.S. Patent Application Publication 2004/0264479 to Raghunandan discloses a method for generating a trie having a reduced number of trie blocks.
- U.S. Patent 7,249,149 to Eatherton et al discloses tree bitmap data structures and their use in performing lookup operations.
- U.S. Patent Application Publication 2004/0111440 to Richardson et al discloses a method for increasing storage capacity in a multi-bit trie-based hardware storage engine by compressing the representation of single-length prefixes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert C. Scheibel whose telephone number is 571-272-3169. The examiner can normally be reached on Mon and Thurs (6:30-5:00) and Fri (6:30-12:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing F. Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RCS 2-19-08

Robert C. Scheibel
Patent Examiner
Art Unit 2619

2/19/08

WING CHAN
SUPERVISORY PATENT EXAMINER